7. SUBJECT DETAILS

7.6 MICROPROCESSORS AND INTERFACING

7.6.1 Objective and Relevance

7.6.2. Scope

7.6.3 Prerequisites

7.6.4 Syllabus

i. JNTU

ii. GATE

iii. IES

7.6.5 Suggested Books

7.6.6 Websites

7.6.7 Experts' Details

7.6.8 Journals

7.6.9 Findings and Developments

7.6.10 i. Session Plan

ii. Tutorial Plan

7.6.11 Student Seminar Topics

7.6.12 Question Bank

i. JNTU

ii. GATE

iii. IES

7.6.1 OBJECTIVE AND RELEVANCE

A handful of additional and less complex chips connected to the microprocessor enable a complete microcomputer to be built. This course provides a comprehensive coverage of the Intel 8086 microprocessor, it's major functional components, memory structure, register structure, instruction set, external interfaces, modes of operation, assembly language programming and introduces architectural concepts and programming of 8051 microcontroller.

7.6.2 SCOPE

Microprocessor technology is an exciting, challenging and growing field which wills private industry for decades to come. Ever since the invent of first microprocessor to the latest, microprocessors have been used in different applications. To meet the challenges of this growing technology, one has also to be familiar with programming aspects of the microprocessor and microcontrollers. This course of microprocessor and interfacing presents an integrated approach to hardware and software in the context of 8086 microprocessor and 8051 microcontroller.

7.6.3 PREREQUISITES

Requires the knowledge of number theory,Boolean algebra, switching theory and logic design and fundamentals of computer architecture.

7.6.4 SYLLA BUS

i. JNTU

UNIT – I: 8 bit / 16 bit Microprocessor:

OBJECTIVE
Upon completion of this unit the students will know the internal architecture of 8085, 8086 along with registers and flags, addressing modes of 8086 and instructions set of 8086.

SYLLABUS
An overview of 8085, Architecture of 8086 Microprocessor Special functions of General purpose registers. 8086 flag register and function of 8086 Flags, Addressing modes of 8086, instruction set of 8086. Assembler directives,simple programs, procedures and macros.

UNIT-II: Assembly level programming:

OBJECTIVE
The student can understand and write an assembly language programmes for microprocessor applications.

SYLLABUS
Assembly language programs involving logical, Branch & Call instructions, sorting, evaluation of arithmetic expressions, string manipulation.

UNIT – III: Modes of Operation in 8086:

OBJECTIVE
The student can learn about instruction executions and interfacing memory devices like RAM,ROM and DMA.

SYLLABUS
Pin diagram of 8086 -Minimum mode and Maximum mode of operation. Timing diagram, Memory interfacing to 8086 (Static RAM and EPROM), Need for DMA. DMA data transfer method, interfacing with 8237/8257.

UNIT – IV: I / O Interface:

OBJECTIVE
The students can learn about the modes of operation of 8255, timing diagram and interfacing of various peripheral devices like A/D, D/A converters and Stepper motor through 8255.

SYLLABUS
8255 PPI- various modes of operation and interfacing to 8086, Interfacing keyboard, displays, Stepper motor and actuators, D/A and A/D converter interfacing.

UNIT – V: Interrupt Control:

OBJECTIVE
The students can understand the interrupt structure of 8086 and internal architecture of 8259 programmable chip.

SYLLABUS
Interrupt structure of 8086.Vector interrupt table. Interrupt service routines. Introduction to DOS and BIOS interrupts. 8259 PIC Architecture and Interfacing, cascading of interrupt controller and its importance.

UNIT – VI: Serial Communication control:

OBJECTIVE
The student can know about serial communication control chips and its interfacing with 8086 microprocessor.

SYLLABUS
Serial data transfer schemes. Asynchronous and Synchronous data transfer schemes.8251 USART architecture and interfacing, TTL to RS232C and RS232C to TTL conversion. Sample program of serial data transfer. IEEE 488 GPIB.

UNIT – VII: Introduction to Microcontrollers:

OBJECTIVE
The student can familiar with the internal architecture of 8051 microcontroller and its assembly language programmes.

SYLLABUS
Overview of 8051 Microcontroller Architecture, I/O ports, Memory organization, addressing modes and instruction set of 8051, simple programs.

UNIT – VIII: Real time control:

OBJECTIVE:

The student can understand the Real time control of 8051 microcontroller and its interrupt structure.

SYLLABUS
Timer/ Counter operation in 8051,Serial communication control in 8051, interrupt structure of 8051, memory and I/O interfacing of 8051.

ii. GATE SYLLABUS

UNIT – I
An overview of 8085

UNIT – II to UNIT-VIII
Not applicable

iii. IES SYLLABUS

UNIT – I
An overview of 8085

UNIT – II to UNIT-VIII
Not applicable

7.6.5 SUGGESTED BOOKS

TEXT BOOKS

T1. Advanced Microprocessors and Peripherals, I.K. Ray and K.M. Bhurchandi , TMH, 2000
T2. Micro Controllers - Ajay V. Deshmukh, Tata McGraw Hill Edition, 2005.

REFERENCE BOOKS

R1. Microprocessors and Interfacing, Douglas V. Hall , 2007.
R2. The 8088 and 8086 Micro Processors: Programming, Interfacing, Software, Hardware and Aplications - Walter. A. Triebel, Avatar Singh, N. .K. Srinath, 2007 Pearson.
R3. Micro Computer System 8086/8088 Family Architecture, Programming and Design - By Liu and GA Gibson, PHI, 2nd Ed.,
R4. Microprocessors, Interfacing and Applications, Ramsingh and II.P. Singh, New Age Publishers
R5. The Intel Microprocessors 8086/8088, 80186/80188, 80286, 80386, 80486, Pentium, and Pentium Pro Processor, Architecture, Programming and Interfacing, Barry ii. Brey, PHI. IV Edn
R6. Microprocessors Principles and Applications, Gillmore, TMH. II Edn
R7. The 8086/ 8088 Family, John Uffenbeck , PHI
R8. 8051 Microcontroller, Kenneth J. Ayala, Penram International, Thomson, 3rd Edn, 2005

7.6.6 WEBSITES

1. www.deas.harvariv.edu/
2. www.manchester.aiii.uk/research/areas/
3. www.eecs.umich.edu/eecs/research/resprojects.html
4. www. kabuki.eecs.berkeley.edu/papers.html
5. www.intel.com
6. www.bbdbestofvi.com/importers
7. www.ecv.uiuiii.edu
8. www.pearsoneiv.co.uk
9. www.atmel.com

7.6.7 EXPERTS' DETAILS

INTERNATIONAL

1. Mr. Kanada Ghose
   University of Newyork, Birmingham
   email : ghose@cs.birmingham.edu

2. Mr. Michel Dubois
   University of Southern California
   email : dubois@paris.usiii.edu

3. Mr. R.Sangireddy
   University of Texas
   email : rami.sangireddy@utdallas.edu

NATIONAL

1. Mr. Preeti Ranjan Panda
   Department of Computer Science and Engineering
   Indian Institute of Technology, Delhi
   Phone: +91-11-2659-6030
   email :panda at csv.iitiv.aiii.in

2. Dr. Jyotinder Singh Sahambi
   Department of Electronics and Communication Engineering
   Phone(Off) : +91-361-258-2510
   email :jsahambi[AT]iitg.ernet.in

3. Prof. S Mukhopadhyay
   Dept. of Electrical Engineering
   IIT Campus, Kharagpur 721302
   Phone (office) +91 - 3222 – 283066
   email :smukh @ev.iitkgp.ernet.in

REGIONAL

1. Provi. R. Govindarajulu
   IIIT, Hyderabad
   email: gregeti@iiit.net

2. Mr. M.II. Srinivas
   IIIT, Hyderabad
   email :srinivas@iiit.net

7.6.8 JOURNALS

INTERNATIONAL

1. IEEE Transactions on Microprocessors and Microsystems
2. IEEE Micro Magazine
3. Embedded Systems Design

NATIONAL

1. IETE Journal of Research
2. IETE Journal of Education

7.6.9 FINDINGS AND DEVELOPMENTS

1. Design of M2M based scalable cost effective remote monitoring system, Vibhute pritish M.,pawer S.S,. Journal of Embedded Systems & Applications, Sept /Dec. 2013, Vol.1,Issue 3, ISSN 2321 – 8533,Pg No. 1 to 9.

2. Energy efficiency is the new fundamental limiter of processor performance, way beyond numbers of processors, Shekar Borkar, Andrew A. Chien, communications of the ACM, Vol.54, Nos, pages 67-77, April 2011.

3. Thermal Balancing policy for multiprorcessor stream computing plat forms, Fabrinzio Mulas, David Atienza, Luca Benini, IEEE Transactions on Computer-Aided design of integrated circuits and systems, Vol.28, No.12, December 2009.

4. ICOs: A model based user interface description technique dedicated to interactive systems addressing usability, reliability and scalability, David Navarre, Eric Barboni, ACM Transactions on Computer-Human interaction, Vol.16, No.4, Artcile 18, November 2009.

5. Nano Electrostatic discharge, Steven, H. Voldman, IEEE Nanotechnology magazine, September 2009.

6. Efficient exact scheduability Tests for fixed priority Real-Time systems. Robert I. Davis, Attila Zabos and Alan Burng, IEEE Transactions on computers, Vol57, No.9, Pg. No. 1261 to 1276, Sept 2008.

7. Photonic Networks-on-chip for future generations of chip multiprocessors, Assaf sacham, Koren Bergman, Lucca P. Carloni, IEEE transactions on computers, Vol.57, No.9, Pg. No.1246 to 1260, Sep 2008

7.6.10 i. Session Plan

Sl. No.	Topics in JNTU Syllabus	Modules & Sub modules	Lecture No.	Suggested Books	Remarks
UNIT –I 8 bit / 16 bit Microprocessor					
1	An over view of 8085	Objective, relevance, pre-requisite and background of micro processor Study of 8085 micro processor	L1	T1-Ch1, R1-Ch1 R3-Ch1, R4-Ch1	IES, GATE
2	Architecture of 8086 Register set of 8086	Introduction of 8086 What is microprocessor General block diagram study BIU and the role of each internal component	L2	T1-Ch1, R1-Ch1 R7-Ch2, R3-Ch2 R5-Ch2, R6-Ch4 R6-Ch5	IES, GATE

3	Special functions of general purpose registers Flag register and Function of each flag	EU and the role of each internal component	L3	T1-Ch1, R1-Ch1 R7-Ch2, R3-Ch2 R5-Ch2, R6-Ch4 R6-Ch5	
		General purpose registers Flag register	L4		
4	Addressing modes of 8086	1) Various types of addressing modes 2) Examples of addressing modes	L5	T1-Ch2, R1-Ch2 R3-Ch2, R5-Ch3 R6-Ch6	
5	Instruction set of 8086	Introduction, Types Data transfer instructions	L6	T1-Ch2,R7-Ch2 R3-Ch3, R5-Ch4	
		String instructions			
		Logical instructions Arithmetic instructions	L7	T1-Ch2, R7-Ch2 R3-Ch3, R5-Ch5	
		Transfer of control instructions Processor control instructions			
6	Assembler directives	Different directives used in programming	L8	T1-Ch2, R3-Ch3	
7	Simple assembly language programming of 8086 involving looping	Programs involving looping Simple programs	L9	T1-Ch3, R3-Ch3 R5-Ch5,7	
8	Procedures	Discuss on sub programs Procedure types	L10	T1-Ch4, R1-Ch5 R7- Ch4	
		Methods of passing parameters			
9	Macros	What is macro Use of macro	L11	T1-Ch4, R1-Ch5 R7- Ch4	

Sl. No.	**Topics in JNTU Syllabus**	**Modules & Sub modules**	**Lecture No.**	**Suggested Books**	**Remarks**
UNIT – II Assembly level programming					
10	Assembly language	Programs using branch instructions	L12	T1-Ch3, T5-Ch3	

	programs involving logical, branch and call instructions	Programs using call instructions	L13	R3-Ch5, R3-Ch7	
11	Sorting	1) Ascending 2) Descending	L14	T1-Ch3, T5-Ch3 R3-Ch5, R3-Ch7	
12	Evaluation of arithmetic expression	Discuss programs to evaluate an arithmetic expression 1) Binary operations 2)BCD operations	L15 L16	T1-Ch3, T5-Ch3 R3-Ch5, R3-Ch7	
13	String manipulation	Programs on string manipulation 1) Display string 2) Verify Password	L17 L18	T1-Ch2, R1-Ch5,6 R7-Ch2, R3-Ch4	
UNIT – III Modes of Operation in 8086					
14	Pin diagram of 8086 Minimum mode and Maximum mode of operation	1)Pin diagram – 8086 2)Minimum mode of operation	L19	TI-Ch1, R7-Ch6 R3-Ch8, R5-Ch8	
		3)Maximum mode of operation	L20	TI-Ch1, R7-Ch6 R3-Ch8, R5-Ch8	
15	Timing diagram	1)Different timing diagrams Read or write in minimum mode 2)Read or write in maximum mode	L21	T1-Ch1, R7-Ch7 R3-Ch8, R5-Ch8	
16	Memory interfacing (Static RAM & EPROM)	Introduction to memories: 1)SRAM interfacing	L22	T1-Ch5, R7-Ch7 R5-Ch9	
		2)EPROM interfacing	L23	T1-Ch5, R7-Ch7 R5-Ch9	
17	Need for DMA DMA data transfer Method	Introduction 1)Block diagram of 8237	L24	T1-Ch7, R3-Ch9 R5-Ch12	
		2)Pin diagram of 8237	L25	T1-Ch7, R3-Ch9 R5-Ch12	
18	Interfacing with 8237/8257	Interfacing of 8237 to 8086 and programming	L26	T1-Ch7, R3-Ch9 R5-Ch12	

UNIT – IV I / O Interface					
19	8255 PPI various modes of operations and interfacing to 8086	Introduction to interfacing 1)Block diagram of 8255	L27	T1-Ch5, R1-Ch9 R3-Ch9, R5-Ch10	
		2)Various Modes of 8255	L28	T1-Ch5, R1-Ch9 R3-Ch9, R5-Ch10	
20	Interfacing of keyboard	1)Interfacing of switches 2)Interfacing of keyboard	L29	T1-Ch5, R1-Ch9	
21	Displays	1) interfacing of LED's 2) interfacing of 7-segment display units	L30	T1-Ch5, R1-Ch9	
22	Stepper motor and actuators	1)Stepper motor interfacing and 2) Actuators programming	L31	T1-Ch5, R1-Ch9	
23	D/A and A/D converter interfacing	Discussion on 8-bit DAC's and its interfacing	L32	T1-Ch5, R1-Ch10 R3-Ch10	
		Discussion on 8-bit ADC's and its interfacing	L33		
UNIT – V Interrupt Control					
24	Interrupt structure of 8086,Vector interrupt table	Introduction 1)Interrupt types 2) Interrupt vector table	L34	T1-Ch4, R5-Ch11	
25	Interrupt service routines	Interrupt service routine programmes	L35	T1-Ch4, R5-Ch11	
26	Introduction to DOS and BIOS interrupts	DOS interrupt BIOS interrupt	L36	T1-Ch4, R5-Ch11	
27	8259 PIC architecture and interfacing	Pin diagram of PIC Block diagram description	L37	T1-Ch6, R7-Ch9 R3-Ch8, R5-Ch11	
		8259 interfacing and programming	L38		

28	Cascading of interrupt controller and its importance	1)Cascading of interrupt controller 2)Applications	L39	T1-Ch6, R7-Ch9 R3-Ch8, R5-Ch11	
UNIT – VI Serial Communication control					
29	Serial data transfer schemes Asynchronous and synchronous data transfer schemes	Introduction to serial communication 1)Asynchronous 2)Synchronous	L40	T1-Ch6, R1-Ch14	
30	8251 USART architecture and Interfacing to 8086	Introduction to 8251 1)Block diagram of 8251 2)Pin diagram of 8251	L41	T1-Ch6, R7-Ch9 R3-Ch9	
		Interfacing of 8251 with 8086 and programming	L42	T1-Ch6, R7-Ch9, R3-Ch9	
31	TTL to RS 232C and RS 232C to TTL conversion	Characteristics of RS 232C 1)TTL to RS 232C and 2)RS232C to TTL	L43	R7-Ch10, R3-Ch9	
32	Sample programs of serial data transfer	Serial data transfer programmes 1) Keyboard 2) Display unit	L44	T1-Ch6, R1-Ch14	
33	IEEE 488 GPIB	Universal serial bus IEEE488	L45	T1-Ch6, R1-Ch14	
UNIT - VII Introduction to Microcontrollers					
34	Overview of 8051 Microcontroller :Architecture	1)Introduction to microcontroller 2) Architecture of 8051	L42	T1-Ch17 R8-Ch3	
35	I /O ports	1)Types of I/O ports 2)Explanation of ports	L43	T1-Ch17 R8-Ch3	
36	Memory organization	1)Types of memories 2)RAM AND ROM	L44	T1-Ch17	

				R8-Ch3	
37	Addressing modes	1)Types of addressing modes 2)Examples of each addressing mode	L45	T1-Ch17 R8-Ch5	
38	Instruction set of 8051	1)Types of Instruction set 2)Explanation of instruction set	L46	T1-Ch17 R8-Ch5	
39	Simple programmes	1)programmes on Arithmetic operations 2)Programmes on Logical operations	L47	T1-Ch17 R8-Ch5	
UNIT - VIII Real time control					
40	Timer/Counter operation in 8051	1)Introduction 2)Timer operation mode 3)Counter operation mode	L48 L49	T1-Ch17 R8-Ch3	
41	Serial communication control in 8051	Serial communication control in 8051 1)Asynchronous data format 2)Synchronous data format	L50	T1-Ch17 R8-Ch3	
42	Interrupt structure of 8051	1)Types of Interrupts 2) Explanation of Interrupts	L51	T1-Ch17 R8-ch3	
43	Memory interfacing of 8051	1)Memory mapping and 2)interfacing of 8051	L52	T1-Ch17 R8-Ch3	
44	I/O interfacing of 8051	1)I/O addresses 2)Interfacing to 8051	L53	T1-Ch17 R8-Ch3	

ii. Tutorial Plan:

Tutorial 1: Calculation of Physical and Logical addresses.

Tutorial 2: Assembly language programs for BCD/Signed operations.

Tutorial 3: Assembly language programs for string manipulations.

Tutorial 4: Timing diagram for minimum and maximum mode

Tutorial 5: Interfacing of display and keyboard with 8086

Tutorial 6: Interfacing of ADC & DAC programmes.

Tutorial 7: Interfacing of 8259 & 8257 with 8086.

Tutorial 8: Interfacing of 8251 with 8086

Tutorial 9: Programs on Serial communications.

Tutorial 10: Programs on BCD operations using Microcontroller

Tutorial 11: Programs on string operations using Microcontroller

Tutorial 12: Problems on Memory interfacing.

7.6.11 STUDENTS' SEMINAR TOPICS

1. Design of microcontroller based automated power system for classrooms. Monzoor G.Ahmed,Natique Z.Khan, Journal of Embedded Systems & Applications, May /Aug. 2013, Vol.1,Issue 2, ISSN 2321 – 8533,Pg No. 9 to 16.
2. A Digital microfluidic approach to chip cooling, Philip Y. Paik, Krishnendu Charabarty, Vasee K. Pamula, IEEE Desing & Test of computers, July /Aug. 2008, Pg No. 372 to 381
3. Microcontroller based Telephone operated Device control Electronics Maker, SSD flash based Hard drive Alternative, October 2008, Issue 149, No.13
4. Microcontroller based commuication between PC & Sony IV IR Remote control, Electronics maker, SSD Flash based Hard Drive Alernative, Octoer 2008, Issue 149, No.13
5. Embedded Application development system for 8051 Microcontrollers, Electronics Maker, Embedded systems, A Multi Billion Industry, August 2007 issue 135, No.12
6. ARM Processor based flash MCU, Electronics Maker, Embedded systems, A Multi Billion Industry, August 2007 issue 135, No.12
7. E- Nose based Ador analysis system, Electronics Maker, Embedded systems, A Multi Billion Industry, August 2007 issue 135, No.12
8. Moving message Dot Matrix display, Electronics Maker, Embedded systems, A Multi Billion Industry, August 2007 issue 135, No.12
9. Microcontroller based adjustable kitchen times system, Home monitoring, Electronics Maker, Embedded systems, A Multi Billion Industry, August 2007 issue 135, No.12
10. Embedded system design using R8C/Tiny microcontroller, Electronics Maker, Embedded systems, A Multi Billion Industry, August 2007 issue 135, No.12
11. Electronics circuit design by simulation software, Electronics Maker, Embedded systems, A Multi Billion Industry, August 2007 issue 135, No.12

7.6.12 QUESTION BANK

UNIT – I

1. a) Compare the salient features of 8085 and 8086 micro processors.
   b) Explain the various addressing modes of 8086 microprocessors. **(Nov/Dec 13)**

2. a) What is the major difference between architecture s of 8085and 8086, Explain.
   b) Explain the function of DAA and HALT instruction with an example. **(Nov/Dec 13)**

3. i. Explain the function of the following signals of 8086.
   (i) ALE, (ii) (iii) HOLD, (iv) NMI,
   (v) , (vi) , (vii) READY, (viii)
   ii. Explain the physical address formation in 8086. **(May 11)**

4. What is meant by an addressing mode? Explain the different addressing modes supported by 8086 with suitable examples. **(May 11)**

5. i. What is an assembler directive? Explain the following assembler directives:
   (i) ASSUME, (ii) EQU, (iii) LABEL, (iv) OFFSET
   ii. Draw the register organization of 8086 and explain typical applications of each register. **(May 11)**

6. i. What are the different instruction types of 8086?
   ii. Explain the following instructions of 8086 with suitable examples:
   (i) LEA, (ii) CMP, (iii) DAA, (iv) CBW (v) MUL, (vi) RCR, (vii) CMC, (viii) JBE **(May 11)**

7. i. What is the difference between HALT state and HOLD state? Discuss the status of different control pins of 8086 in both the states?
   ii. Explain how an 8086 enters into Wait State? How many wait states can be inserted in a machine cycle? **(May 09)**

8. i. What is the purpose of ALE, BHE, DT/ and pins of 8086? Show their timing in the system bus cycle of 8086?
   ii. Why 8086 memory is mapped into 2 byte wide banks? What logic levels are found with BHE and A0 when 8086 reads a word from the address 0A0AH? **(May 09)**

9. i. What is the purpose of ALE, BHE, DT/ and pins of 8086? Show their timing in the system bus cycle of 8086?
   ii. Show the complete design to generate system address, data and control buses using the above pins, latches and transceivers.? **(Nov 09)**

10. i. What is a recursive procedure? Write a recursive procedure to calculate the factorial of number N, where N is a two digit Hex number
    ii. What are the loop instructions of 8086? Explain the use of DF flag in the execution of string instructions? **(May 09, Sep 08)**

11. i. Write in detail about the addressing modes of 8086 Microprocessor
    ii. What are procedures? Give examples. **(May 09)**

12. i. Describe the following addressing modes with some examples.
    a. Indexed addressing with displacement
    b. I/O port addressing
    ii. Explain the meaning of the following 8086 instructions
    a. mov [3845h], bx
    b. add ax, [si]
    c. mov bx, 2956h
    d. adc ax, bx **(May 09)**

13. i. Explain in detail about the following addressing modes of 8086 with examples.

a. I/O port addressing
b. Based indexed addressing with displacement

ii. Write an ALP in 8086 to add two 16- bit hexa decimal numbers **(May 09)**

14. i. What are the loop instructions of 8086? Explain the use of DF flag in the execution of string instructions.
ii. Give the assembly language implementation of the following.
a. IF-THAN-ELSE
b. REPEAT **(May 09)**

15. i. Discuss various branch instruction of 8086 microprocessor, that are useful for relocation?
ii. Using a do-while construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again. **(May 09)**

16. i. Give the 8085 compatible flags of 8086 processors? Discuss the design of each flag?
ii. List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment? **(May 09,Sep 08, 07)**

17. Explain the function of following registers in 8086 microprocessor :
i. AX,BX,CX,DX
ii. CS,DS,SS,ES
iii. BP,SP,SI,DI
iv. IP and Instruction Queue **(May 09)**

18. i. Draw the architectural diagram of 8085 and explain the function of each block in detail
ii. Discuss about Multiplexing in 8086 microprocessor **(May 09)**

19. i. With a neat architectural diagram explain the functioning of an 8086 microprocessor
ii. Compare the flag resisters of 8086 & 8085 **(May 09)**

20. i. Explain why 8086 internal architecture is divided into BIU and EU? Discuss the A-bus, B-bus and C-bus and their use?
ii. Explain the difference between memory segmentation and memory page? Why segmentation is useful in real-time applications? **(May 09)**

21. i. What is the purpose of addressing mode? It is necessary to move a byte from location 5000H:0102H to 5000H:0050H. Give all possible methods using 8086 addressing modes?
ii. Explain the use of Direction flag and Interrupt flag with examples? **(May 09)**

22. i. Compare 8 bit processors and 16 bit processors from the architectural view.
ii. Explain overflow condition with 8 bit signed data. Generating overflow flag using other flags of 8086? **(Sep, Aug 08)**

23. i. Explain various interrupts of 8085 Microprocessor and their functionality? **(Apr 08)**
ii. Explain the
a. SID
b. SOD
c. S0, S1, S2
iv. INTA pins of 8085 Microprocessor.

24. i. Explain in detail the coding template for ADD instruction of 8086. **(Apr 08)**
ii. It is necessary to declare a program as a public procedure to be accessible by other programs? Give the sequence of assembly language statements? An external program called “fact” is to used in this program. Show the required statements?

25. i. Explain the flag register of 8086. **(Apr 08)**
ii. Explain the concept of memory segmentation.
iii. Explain, when Queue is failing to speed up the execution.

26. i. Draw the internal architecture of 8085? Explain about each block in it. **(Apr 08)**
ii. Explain the function of OPCODE pre fetch FIFO Buffer in 8086?

27. Explain the following instructions and their use? **(Apr 08)**
a. LODSB
b. CMPSW
c. XLAT.

28. i. Explain the functions of different registers in 8086. Also discuss the flag register contents. **(Apr 08)**
ii. How procedure CALL and RET take place in 8086. Explain conditional and unconditional CALL and RET instructions in 8086 instruction set.

29. i. Write a program to move a block of memory with out over lapping. **(Apr 08, Sep 07)**
ii. Discuss the following instructions.
a. ADC
b. AAS
c. IMUL
d. CBW.

30. i. List out the major steps in developing an assembly language program. **(Sep 07)**
ii. What are the main advantages of top-down design approach?

31. i. Explain the various addressing modes used in 8086. **(Sep 07)**
ii. Explain the different types of Instruction Formats used in 8086.

32. Explain clearly with examples the following 8086 instructions. **(Sep 07)**
i. REP prefix
ii. XLAT
iii. IN and OUT
iv. MOV
v. ADD AX, ES:[SI]
vi. PUSH.

33. The register contents of 8086 is given below. CS=5000H, DS=8000H, SS=9000H,ES=7000H, SI=1000H, DI=2000H, BP=0008H, SP=0002H, AX=0000H, BX=5200H,CX=8000H, DX=2800H Calculate the effective address and physical address for different addressing modes of 8086 microprocessor by assuming suitable Instructions. **(Sep 07)**

34. List out the assembler directives of 8086? And explain them with Examples?

35. i. Draw the block diagram of 8086 and explain the functions of GPRs? **(Sep 07)**
ii. Discuss the function of segment registers of 8086 with examples?

36. i. Explain various parts of BIU in 8086. **(Sep 07)**
ii. Explain following instruction Formats with examples.
i. One byte instruction, register mode.
ii. Register to / from memory with no displacement.

37. i. Explain the architecture of 8085 microprocessor with a neat block diagram.
ii. What is an instruction? Explain various instruction formats with examples **(Sep 07)**

38. i. Explain what are the advantages of the memory segmentation. Discuss About various segment registers in 8086.
ii. Explain the physical memory organization in 8086. How is it differ from 8088 **(Sep 07)**

39. i. Draw the internal architecture of 8085? Explain each block.
    ii. What are the special functions of GPRs in 8086? And explain them? **(Sep 07)**

40. i. What is the length of the instruction queue in 8086? Discuss the use of the queue? Explain the reason for limiting the length of queue?
    ii. What is the minimum number of segment resisters that are necessary to provide segmentation? How do you access common data for different programs using segmentation? **(Sep 07)**

41. i. Draw the block diagram of 8086 and explain each block?
    ii. Discuss the addressing modes provided by 8086 and explain with examples? **(Sept, Apr 06)**

42. Using DF flag and string instructions, write an assembly language program to move a block of data of length N from source to destination. Assume all possible conditions. **(Sept, Apr 06)**

UNIT – II

1. a) Explain different ways of passing parameters to subroutine.
   b) Explain the functions of the following pins.
   i) *MN MX* ii) HLDA iii) *DT R* iv) ALE **(Nov/Dec 13)**

2. a) Write an 8086 assembly language program for arranging elements of an array in descending order.
   b) Given that (IP) = 2BCO, (CS) = 0200, Displacement = 5119, (BX) = 1200,(DS) = 212A, (224A0) = 0600, (275B9) = 098A.Find the branch address for a branch instruction that uses
   i) Intra segment direct addressing
   ii) Intra segment indirect addressing which uses BX register and register addressing. **(Nov/Dec 13)**

3. i. Write an ALP in 8086 to find a maximum number in the array of 10 numbers.
   ii. Write an ALP in 8086 to add two 16-digit packed BCD numbers. **(May 11)**

4. i. Write an 8086 assembly language program to find the product of two 3 × 3 matrices. The matrices are stored in the form of lists (row-wise). Store the result in the third matrix.
   ii. Write an ALP in 8086 to exchange a block of N bytes of data between source and destination. **(May 11)**

5. i. Write an 8086 assembly language program to arrange a given series of hexadecimal bytes in ascending order.
   ii. Write an 8086 assembly language program for addition of two 3 × 3 matrices. The matrices are stored in the form of lists (row-wise). Store the result of addition in the third list. **(May 11)**

6. i. Write an 8086 assembly language program to find out the number of positive numbers and negative numbers from a given series of signed numbers.
   ii. Write an 8086 assembly language program to convert a 16-bit binary number into equivalent BCD number. **(May 11)**

7. It is necessary to check weather the word stored in location 6000H:6000H is zero or not. Show all possible ways of testing the above condition using direct addressing modes and store 0FFH if the condition is satisfied in location A000H:1002H. Otherwise store 00H. **(Nov 09)**

8. It is necessary to check weather the word stored in location A000H:A000H is positive number or not? Show all possible ways of testing the above condition and store 00H if the condition is satisfied in location E000:2002. Otherwise store 0FFH **(Nov 09)**

9. 8086 processor do not provide memory indirect addressing mode. Show all possible ways to access a word from memory where the segment address is given in location C000H:1000H and the o"set is given in location C000H:1002H. Give the instruction sequence for every addressing mode of 8086.? **(Nov 09)**

10. 8086 processor do not provide memory indirect addressing mode. Show all possible ways to access a word from memory where the offset is given in location 3000H:4000H. Use other addressing modes of 8086 and give instruction sequence for every method? **(Nov 09)**

11. It is necessary to check the parity of the data byte in location 4000H:01FEH. If the parity is even store 00H otherwise store 0FFH in location 5000H:1000H. Give the instruction sequence for every addressing mode to achieve the above result. **(May 09)**

12. i. Write an ALP in 8086 to find a maximum number in the array of 10 numbers
    ii. Write a recursive program in 8086 ALP to find the sum of the first "n integers **(May 09)**

13. i. Write an ALP in 8086 to move a block of N bytes of data from source to destination
    ii. Write an ALP in 8086 to add 5 bytes of data in an array by making use of procedure **(May 09)**

14. i. Write a program in 8086 to add two 8-bytes of data available in memory location array1 and array 2. Store the result in array3
    ii. Write an ALP to count number of 0s in a 16 bit binary string **(May 09)**

15. i. Write an ALP in 8086 to add two 16-digit packed BCD numbers
    ii. Write an ALP in 8086 to divide a 32-bit number by a 16-bit number **(May 09)**

16. Write a recursive routine to evaluate the following polynomial
Y = A0+A1X1+A2X2+A3X3+....+ANXN. The coefficients A0, A1, A2....AN are to be successive words in memory and all parameter addresses are to be passed via the stack. **(Apr 08)**

17. Write an algorithm and assembly program to sort the numbers in an array in descending order using bubble sort method **(Apr 08)**

18. i. Write a program to sort an array in descending order. **(Apr 08)**
    ii. Give the instruction sequence that compares the first 20 bytes beginning at STRG 1with the first ten bytes beginning at STRG 2 and branches to MATCH if they are equal, otherwise continues in sequence? **(Apr 08)**

19. i. Write an assembly language program that will examine an ASCII string of 100 characters and replace each decimal digit by a %. The character string starts at STRG. **(Apr 08)**
    ii.. Explain the prefix instruction format of 8086 processor? Discuss how these instructions are useful in string manipulation?

20. i. Write an ALP to move the contents of a block of memory to another area In the memory. (Assume no over lapping).
    ii. What is a stack? Explain 8086 instructions for pushing and popping data on stack. **(Sep 07)**

21. i. Explain string instructions supported by 8086 processor? **(Sep 07)**
    ii. Give the instruction sequence that compares the first 10 bytes beginning at STRG1with the first ten bytes beginning at STRG 2 and branches to MATCH if they are equal, otherwise continues in sequence?

22. Write an algorithm and assembly program for a cash bill of n materials. Rupees are a 4 digit and paisa is a 2 digit number which are stored in two different arrays. Find the total amount for the n materials. Subtract 10% discount on the total and give the actual amount to be parity. Hint Shift the total amount by one digit to get the 10% discount and get the actual amount. **(Sep 07)**

23. i. Write an 8086 assembly language program to check the password of length 4 bytes entered through key board whether it is matching with the system pass word stored from FFOOH location.
    ii. Develop a sequence of instructions that scan through a 300 H byte section of memory called LIST located in the data segment searching for a 66 H. **(Sep 07)**

24. i. Using Loop instruction write a sequence to add two 16 digits 10's Complement packed BCD numbers. Repeat for unpacked BCD numbers.
    ii. Explain with illustrations conversion of an ASCII- coded decimal number Into its binary equivalent **(Sep 07)**

25. i. Consider a string of characters stored in STRING through STRING+99. Suppose that bit 5 of register DL is to be set to 1 if the string contains a digit; otherwise this bit to be set to zero .In any case only bit 5 is to be affective. Draw a flow chart of the problem and implement it in assembler language.
    ii. Write a program sequence for interchanging the contents of two locations. **(Sep 07)**

26. Write a FAR procedure SER WORD that searches a word array for a given word and sets the value of a word parameter to the index of the element in the array if a match is found; otherwise, it puts a -1 in the index word parameter. The parameters are to be passed to the procedure via a parameter address tablv. Give a sequence for calling SER WORD to search ARRAY1 of length LENGTH1 for variable ID? and put the index in INDEDX 1? **(Sep 07)**

27. Develop an 8086 assembly language program that reads a key from the keyboard and converts it to uppercase before displaying it. The program need to terminate, on typing the control C key. **(Sep 07)**

28. i. Write an algorithm and assembly program to convert a 16 bit number to a maximum of 5 unpacked digits.
    ii. Write an algorithm and assembly program to convert an unpacked 4 digit BCD number to Binary number.

29. It is necessary to check whether the word stored in location 4000H:A000H is positive number or not? Show all possible ways of testing the above condition and store 00H if the condition is satisfied in location 3000:2002. Otherwise store 0FFH. **(Sept 06)**

30. It is necessary to define a block of data in 8086 assemble language program. The length of the block is 90,000 Bytes. Give the initialization of data segment for the above block of data? It is necessary to add second element and 68000th element of the above data. Give the sequence of instructions to perform the above operation? **(Sept 06)**

31. i. Discuss various branch instruction of 8086 microprocessor, that are useful for relocation?
    ii. Using a do-while construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again. **(Apr 06)**

32. It is necessary to define a block of data in 8086 assemble language program. The length of the block is 80,000 Bytes. Give the initialization of data segment for the above data? It is necessary to exchange second element and 70000th element in the above. Give the sequence of instructions to perform the above operation? **(Apr 06)**

33. i Develop an 8086 assembly language program to compute nCr using recursive procedure. Assume n and r to be positive integers and place the binary result in a memory world location.
    ii Write an 8086 assembly language program to convert each byte of the code received from IBM PC to SDK 8086 Board, to ASCII codes for the nibbles in the byte. Use IF-THEN-ELSV.(eg:- 7AH received is sent as 37H, the ASCII code for 7 and 41 for A). **(Mar 06)**

34. Develop an 8086 assembly language program to find the LCM of two 16-bit unsigned integers.**(Mar 06)**

35. Write an 8086 assembly language program which adds a byte number from one memory location to a byte from the next memory location, puts the sum in a third memory location, and saves the state of the carry flat in the least significant bit of a fourth memory location mask the upper 7 bits of the memory location where the carry is store. **(Nov 05)**

36. Write an 8086 assembly language program to check the password of length 4 bytes entered through key board whether it is matching with the system password stored at FF00H location. **(Nov 05)**

37. Write an 8086 ALP to insert a substring into a main string which has to be sorted and then suitably insert. **(Nov 04)**

38. Write an 8086 program to delete a substring from a main string whose starting data base is 6DH and ends with OOH. Also give the new length of the string after deletion. **(Nov 04)**

39. i. Add two 5 byte numbers such that the sum is stored in one of the source array locations.
ii. Write an 8086 ALP to convert the Fahrenheit temperature to Celsius temperature. **(Nov 04)**

40. Develop an 8086 assembly language program that will determine if a given sub string is present or not is a main string of characters. Place the result as a '1' if present or as 'O' if not present in a memory location.

(May/Jun 04)

41. i. What condition or conditions will terminate the repeated string instruction REPNE SCASB? and also describe what the CAMPSB instructions accomplish?
ii. Develop a sequence of instructions that scan through a 300 H byte section of memory called List located in the date segment searching for a 66 H. **(Nov 04)**

42. i. Distinguish between the inter segment and intra segment CALL instructions and explain how they will be executed with examples.
ii. Draw neatly the basic 8086 system timing (both read and write) diagrams. **(Apr 04)**

UNIT – III

1. a) Write an assembly code to reverse a given string using stack operations.
b) Explain about maximum mode of 8086 with a neat diagram showing transceivers, clock generator and address latches **(Nov/Dec 13)**

2. a) Show the circuit required to generate the upper and lower I/O strobes in minimum and maximum modes of 8086.
b) Explain the need for DMA and DMA data transfer Method. **(Nov/Dec 13)**

3. i. Describe how the control bus signals are produced for an 8086 system operating in maximum mode.
ii. Describe the series of actions that a DMA controller will perform after it receives a request from a peripheral device to transfer data from the peripheral device to memory. **(May 11)**

4. i. What is the major difference between an 8086 operating in minimum mode and an 8086 operating in maximum mode?
ii. Draw and discuss the minimum mode 8086 system with relevant read and write cycle timing diagrams. **(May 11)**

5. i. Explain how static RAMs are interfaced to 8086. Give necessary interface diagram assuming appropriate signals and memory size.
ii. Explain the need of DMA. Discuss in detail about DMA data transfer method. **(May 11)**

6. i. What is the major difference between an 8086 operating in minimum mode and an 8086 operating in maximum mode?
ii. Draw and discuss the maximum mode 8086 system with relevant read and write cycle timing diagrams. **(May 11)**

7. Why do we prefer interrupt driven data transfer than programmed I/O transfer? Show the complete hardware design to resolve the multiple interrupts based on priority? **(May 09)**

8. i. With appropriate pin diagrams explain the minimum and maximum mode operations of 8086.
ii. Explain the need for DMA in Microprocessor based systems. **(May 09)**

9. i. With a neat timing diagram explain how a WRITE operation is performed by 8086
ii. With a neat pin diagram explain the maximum mode operation of 8086 **(May 09)**

10. i. With a neat block diagram explain the working of 8237 DMA controller

ii. Differentiate between static and dynamic RAMs. Give some examples **(May 09)**

11. i. With a neat block diagram, explain the working of 8257 DMA controller
    ii. Explain briefly about memory interfacing with 8086 microprocessor **(May 09)**

12. i. Explain demand transfer mode and block transfer mode of 8237?
    ii. Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
    iii. Explain how memory to memory transfer is performed with 8237? **(May 09)**

13. It is necessary to interface 128KB SRAM and 32KB EPROM to an 8086 based system. The size of SRAM and EPROM chips is 16KB. Address map of SRAM is fixed from 00000H to 1FFFFH and that of EPROM is from F8000H to FFFFFH. Design the entire memory interface? Give the address map of individual chip? **(May 09)**

14. i. Design the required logic to generate read, write control signals for memory and I/O in a target system using 8086 microprocessor? Generate bank select signals for even and odd address memory banks?
    ii. With the help of basic cell explain SRAM and DRAM? Discuss the advantages and disadvantages of the above memories? **(May 09)**

15. i. What is a memory module? Draw the block diagram of SDRAM module and explain each block?
    ii. Why do you need wait states? Explain how wait states are generated?
    iii. Give possible solutions to meet the processor access time requirements when memory is interfaced to the processor? **(May 09)**

16. i. Draw the basic cell structure of EPROM and explain the principle of operation?
    ii. It is necessary to interface 128KB of EPROM in target system with two memory banks, one for even and other for odd addresses. The chip size of EPROM's is 16KB. Design the memory interface using 74LS138 decoder? **(May 09**

17. i. With a neat sketch explain 8237 DMA controller and its operation?
    ii. With the help of basic cell explain SRAM and DRAM? **(Apr 08)**

18. What are the functions of a DMA controller? Explain the various DMA modes. Describe in brief the steps that take place during a DMA Operation. **(Sep 07)**

19. i. What is the purpose of ALE, BHE, DT/R and DEN pins of 8086? Show their timing in the system bus cycle of 8086?
    ii. Write an 8086 ALP to multiply two 8-bit numbers using SHIFT and ADD method. Store the result in DX register **(Sep 07)**

20. i. What are the contents of the data bus and the status of A0 and BHE when the following instructions are executed in 8086?
    a. CPU writes a byte 11 H at memory location 1000H : 0002 H.
    b. CPU writes a word 2211 H at memory location 1000H : 0003 H.
    ii. Write the functions of the following pins of 8086.
    a. MN/ MX
    b. DEN
    c. ALE
    d. Ready.
    iii. Draw a block diagram to interface two 16K X 8 SRAM (62128) to the 16-Bit data bus of 8086 based system. Design the address decoder for the address range from 00000H - 07FFFFH for both the SRAMs.**(Sep 07)**

21. i. What are the registers available in 8257? What are their functions?
    ii. Draw and discuss the status registers of 8257? **(Sep 07)**

22. i. List the signals in minimum and maximum modes. **(Sep 07)**

ii. Explain the roles of pins TEST, LOCK.
iii. Which are the pins of 8086 that are to be connected to interface 8284 and explain their functions?

23. i. How DRAM's are different from SRAM's? Why DRAMs are said to employ address multiplexing?
ii. What are the conditions that will cause EU to enter a 'Wait State'?
iii. What logic levels would you find on BHE and A0:
a. When an 8086 is writing a byte to the memory address 04032H,
b. When it is writing a word to the memory address 04032H. Also, describe the 8086 bus operations required to write a word at memory address 04031h. **(Sep 07)**

24. i. With a neat sketch explain 8237 DMA controller and its operation?
ii. With the help of basic cell explain SRAM and DRAM? **(Sep 07)**

25. i. Show the circuit required to generate the upper and lower I/O strobes in minimum and maximum modes of 8086?
ii. What is the minimum no. of bus cycles that can occur between the time an interrupt request is recognized and the first instruction in the interrupt service routine is feature. Draw the interrupt acknowledge cycle?

(Sept 06)

26. At what time the INTR signal is recognized by 8086 processor? Show the timing diagram assuming that INTR is active? Explain interrupt acknowledge cycle with its associated timing diagram. **(Sept 06)**

27. i. Discuss the system bus cycle of 8086 with a neat diagram? What is the use of wait cycles? Compare wait and idle cycles?
ii. Show the circuit required to generate the upper and lower I/O strobes in minimum and maximum modes of 8086? **(Sept 06)**

28. What is function of ready pin in 8086. Draw the circuit diagram for wait state generation between 0 and 7 wait states and draw the corresponding timing diagram. **(Sept 06)**

29. i. What is the purpose of ALE, BHE, and pins of 8086? Show their timing in the system bus cycle of 8086?
ii. Why 8086 memory is mapped into 2 byte wide banks? What logic levels are found with and A0 when 8086 reads a word from the address 0A0AH? **(Apr 06, Nov 04)**

30. i. Explain demand transfer mode and block transfer mode of 8237?
ii. Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
(Sept 06, Nov 04)

31. Explain how memory to memory transfer is performed with 8237? **(Sept 06, Nov 04)**

32. i. Draw the flowchart showing how synchronous serial data can be sent from a port line using software routine?
ii. Draw the block diagram of 8237 and explain each block. **(Sept 06)**

33. i. Discuss the organization of FLASH memory? Explain the FLASH memory command definitions?
ii. With the help of basic cell explain SRAM and DRAM? Discuss the advantages and disadvantages of the above memories? **(Sept, Apr 06, 04)**

34. i. With a neat sketch explain the function of memory array of PROM?
ii. Draw the basic cell structure of EPROM and explain the principle of opera tion?
iii. Distinguish between EPROM and E2PROM? Mention their application areas? **(Sept 06, Apr 04)**

35. i. Draw the basic cell structure of EPROM and explain the principle of operation?
ii. It is necessary to interface 128KB of EPROM in target system with two memory banks, one for even and other for odd addresses. The chip size of EPROM's is 16KII. Design the memory interface using 74LS138 decoder? **(Sept 06)**

36. i. Explain the following terms with reference to DRAM **(Apr 06)**

a. Write cycle
b. Access time
c. Refresh
d. Read cycle

ii. Design the required logic to generate read, write control signals for memory and I/O in a target system using 8086 microprocessor? Generate bank select signals for even and odd address memory banks?

37. In an SDK-86 kit 128KB SRAM and 16KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 1FFFFH and that of EPROM is from FC000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KII. EPROM chip size is 8KII. Give the complete memory interface and also the address map for individual chips? **(Apr 06)**

38. i. With a neat sketch explain 8237 DMA controller and its operation?
ii. How do we connect RS-232C equipment
a. To data terminal type devices?
b. To serial port of SDK 86, RS-232C connection? **(Apr 06)**

39. What is function of ready pin in 8086. Draw the circuit diagram for wait state generation between 0 and 7 wait states and draw the corresponding timing diagram. **(Apr 06)**

40. Explain the following data transfer schemes.
i. Programmed I/O
ii. Interrupted I/O
iii. DMA **(Apr 06)**

41. i. Why buffers are needed on the address, data, and control buses in a microcomputer system ?
ii. Draw the structure of fully buffered 8086 microprocessor with the de multiplexed address and data buses. **(Apr 05)**

42. i. Explain different modes of DMA transfer supported by 8237?
ii. Draw the block diagram of 8251 and explain each block? **(Apr 05)**

43. What are the different control signals necessary for I/O read and write cycles? Show how these control signals are generated in minimum and maximum modes of 8086? **(Apr 05)**

44. Describe the function of the following pins and their use in 8086 based system.
i. NMI ii RESET **(Apr 05)**

45. Describe memory-mapped I/O and direct I/O. Give the main advantages and disadvantages of each. **(Apr 05)**

46. Show the truth Table for a 3625 PROM decoder to produce CSI signals for 4Kx8 RAMS in an 8086 system. Assume that the first RAM starts at address 00000H. Also draw the circuit connections.**(Apr 05)**

47. Show the truth Table for a 3625 PROM decoder to produce CSI signals for 4Kx8 RAMS in an 8086 system. Assume that the first RAM starts at address 00000H. Also draw the circuit convections.**(Apr 05)**

48. i. Explain the functions of and MN / pins of 8086 in detail.
ii. Explain physical address, effective address, offset used in 8086. **(Nov 04)**

49. i. What are the registers available in 8257? What are their functions?
ii. Draw and discuss the status resisters of 8257? **(Nov 04)**

50. i. Draw and discuss the mode set register of 8257?
ii. Discuss the priorities of DMA request inputs of 8257?
iii. Explain functions of the following signals of 8257?
a. ADSTB b. TC c. HRQ d. AEN **(Nov 04)**

51. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KII. EPROM chip size is 16KII. Give the complete memory interface and also the address map for individual chips? **(Apr 04)**

52. Interface 8K x 8 EPROM to 8086 microprocessor in the address range FE000H to FFFFFH. by using 2732 EPROM chips. **(Apr 04)**

53. Consider a maximum mode 8086 system that is executing the instructions MOV AX , DATA (data has an even address) CMP AX, 1.Suppose that an interrupt request arise while the first instructions is executing and draw. A timing diagram of the bus activity from the beginning of the first instruction until the interrupt type is received by the processor. **(Apr 04)**

54. i An 8086 system has a DMA controller 8257 interfaced such the address of its mode set register is F8H and address of its DMA address register of channel 0 is F0H.
    ii Write an ALP to read 2K bytes of data from location 5000H:200H in the system memory to a peripheral on channel of the DMA controller. Disable all other channels, program TC stop, No auto load is required, fixed priority **(Nov 04)**

55. Describe in detail the bus activity that takes place while two consecutive bytes are transferred from memory to an I/O device over a 16 bit 8086 bus by an 8237 DMA controller. **(Apr 04)**

56. Give a set of instructions that will:
    i. Mask channels 0 and 3 of an 8237.
    ii. Cause a program-initiated DMA transfer on channel 2 of an 8237 according to the current contents of its controls, address, and byte count registers. **(Apr 04)**

57. Describe in detail the bus activity that takes place while two consecutive bytes are transferred from memory to an I/O device over a 16 bit 8086 bus by an 8237 DMA controller. **(Apr 04)**

58. With a neat block diagram explain how the memory is accessed by 8086 microprocessor using address, data buses and the BHE line. **(Apr 04)**

59. What are the important signals of 8086? Discuss them in detail **(June 03)**

60. Distinguish between minimum and maximum modes of operation of 8086 **(Nov 03)**

61. i. What is the advantage of DMA control data transfer over interrupt driven or program control Data transfer? Why are DMA control data transfers faster?
    ii. With a neat flow diagram, explain sequence of operations for DMA data transfer **(Nov 03)**

62. i. Explain with a neat diagram interfacing of 8237 with 8086.
    ii. Write the programming features of 8237 DMA controller **(Nov 03)**

63. Sketch and explain 8086. Read and write bus cycle timing diagrams in minimum mode. **(Nov 02)**

64. i. Explain in detail how basic signal flows on 8086 buses. **(Nov 02)**
    ii. Describe memory-mapped I/O and I/O mapped I/O. Give the main advantage and disadvantage of each

65. Explain the functions of 'READY' pin in 8086. Explain the pipelining in 8086. **(June 03)**

66. Explain clearly 8086 system bus structure. **(Nov 02)**

67. Write short notes on Memory organization of 8086 **(Nov 02)**

68. An 8086 based micro computer in the minimum mode is to be designed to provide 2kx16 EPROM, lkx16 static RAM and six 8 bit I/O ports. **(Nov 02)**

69. i. Use 2716 EPROMs, 2142 static RAMs and 8255 I/O chips. Use suitable decoding circuits and gives a neat detailed diagram showing important signal connections and memory map.
ii. Give the functional block diagram of peripheral IC 8259. Write in brief the programming features of 8259 **(Nov 02)**

UNIT – IV

1.How many types of modes of operations are there in 8255 PPI and explain them. **(Nov/Dec 13)**

2. a) Explain how memory to memory transfer is performed with 8237.
b) Explain the interfacing of an ADC 0808 with 8086 using 8255 ports with a neat interfacing diagram and also write an assembly language program. **(Nov/Dec 13)**

3. i. Draw and explain the stepper motor interface to 8086 and write small program to rotate stepper motor in clock wise and anticlockwise direction.
ii. Explain the A/D converter interface to 8086 microprocessor. **(May 11)**

4. i. Explain the architecture of 8279 keyboard display controller with the help of a neat diagram.
ii. Distinguish between Mode set control word and BSR control word of 8255? **(May 11)**

5. i. Explain the control word format of 8255 in I/O and BSR mode.
ii. Write an ALP in 8086 to generate a symmetrical square waveform with 1KHz frequency? Give the necessary circuit setup with a DAC? **(May 11)**

6. i. What is the sensor matrix mode of 8279? Explain the function of the 8 × 8-bit RAM in this mode.
ii. Explain the function of the following signals of 8279.
(i) SL0 – SL3, (ii) RL0 – RL7, (iii) IRQ, (iv) CNTL / STB **(May 11)**

7. Explain the following data transfer schemes.
i. Programmed I/O
ii. Interrupted I/O
iii. DMA **(May 09,06)**

8. Why do we prefer interrupt driven data transfer than programmed I/O transfer? Show the complete hardware design to resolve the multiple interrupts based on priority? **(May 09)**

9. Explain why 8255 ports are divided into two groups? Discuss how these groups are controlled in different modes of operation? Explain different control signals and their associated pins for bi-directional I/O mode of operation? **(May 09)**

10. i. What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2?
ii. Explain the transistor buffer circuit used to drive 7-segment LEDs **(May 09)**

11. Interface a stepper motor with 8-step input sequence to 8086 based system and write the instruction sequence to move the stepper motor 20 steps in clockwise and 12 steps in anti-clockwise direction. **(May 09)**

12. i. Explain the application of stepper motor in microcomputers?
ii. How do you interface ADC to microprocessor? Give the required instruction sequence to acquire one sample from ADC? **(May 09)**

13. i. Distinguish between Mode set control word and BSR control Word of 8255?

ii. Write an ALP in 8086 to generate a symmetrical square wave form with 1KHz frequency? Give the necessary circuit setup with a DAC? **(May 09)**

14. i. Discuss about following control words of 8255?
    a. Mode Set Control word.
    b. Bit Set/Reset Control word
    ii. Explain about interfacing of a DAC with 8086 using 8255? **(May 09)**

15. i. Distinguish between a system clock and peripheral clock and explain briefly the control block of 8255.
    ii. Explain how an ADC can be interfaced to a microprocessor? Give the required instruction sequence to acquire one sample from ADC? **(May 09)**

16. i. Interface the stepper motor with 8255 and write an ALP to rotate the stepper motor continuously in clockwise direction. **(Apr 08)**
    ii. Write an assembly language program to rotate a 200 teeth, 4 phase stepper motor as specified below: Ten rotations clockwise and eight rotations anticlockwise.

17. Explain the following terms in relation to 8279: **(Apr 08)**
    i. Two key lockout ii. N-key rollover iii. Right entry iv. Left entry v. FIFO
    vi. Display RAM vii. Blanking viii. Key de-bounce.

18. i. Draw the interfacing scheme of 8255 and 8086 in memory mapped I/O mode. **(Apr 08)**
    ii. An 8255 is used with port-A input in mode-1, Port-B as output in mode-1 and with Port-C used for handshaking for Port-A and Port-B. Assume the address of Port-A is 80H.
    a. Determine the control word and write the instruction sequence to program the 8255 for this mode of operation.
    b. Draw the scheme of connections required.

19. Write the necessary instruction sequence to initialize 8255 with address 0200H to 0203H for the following combinations:
    i. Port-A as input port in mode-1 and Port-B as input port in mode-1 with interrupt driven I/O.
    ii. Port-A in mode-2 and Port-B as input port in mode-1 with interrupt driven I/O.
    iii. Port-A as output port in mode-0 and Port-C upper half as input port in mode-0, and Port-B as output port in mode-1 with interrupt driven I/O.
    iv. Port-A as output port in mode-1 with active interrupt, Port-B as output port in mode-0 and Port-C lower half as input port in mode-0. **(Apr 08)**

20. Interface a 12-bit DAC to 8255 with an address map of 0800 H to 0803 H. The DAC provides output in the range of +5V to -5V. Write the instruction sequence.
    i. For generating a square wave with a peak to peak voltage of 2V and the frequency will be selected from memory location "FREQ".
    ii. For generating a triangular wave with a maximum voltage of +5V and a minimum of 0V **(Sep 07)**

21. Briefly explain the interfacing and programming of 8279 **(Sep 07)**

22. i. Explain the control word format of 8255 in I/O mode and BSR mode.
    ii. Interface an 8255 with 8086 so as to have Port-A address BCD1H, Port-B address BCD3H, Port-C address BCD5H and Control word register address BCD7H. **(Sep 07)**

23. i. What is sensor matrix mode of 8279? Describe the function of the 8x8-bit RAM in the sensor matrix mode.
    ii. Interface the keyboard and display controller 8279 with 8086 at address ABC0H. Write an ALP to set up 8279 in scanned keyboard mode with encoded scan, N-key rollover mode. Use 16-character display in right entry display format. **(Sep 07)**

24. i. What is sensor matrix mode of 8279? Describe the function of the 8x8-bit RAM in the sensor matrix mode.

ii. Interface the keyboard and display controller 8279 with 8086 at address ABC0H. Write an ALP to set up 8279 in scanned keyboard mode with encoded scan, N-key rollover mode. Use 16-character display in right entry display format. **(Sep 07)**

25. i. Explain the methods for excitation of stepper motor.
    ii. Interface stepper motor with 8086 microprocessor system and write an assembly language program to rotate it by 1800. **(Sep 07)**

26. i. Interface a 4x4 keyboard using two 8255 ports and write a program to read the code of a pressed key.
    ii. Show the sequence of instructions you can send to the 8279 of the SDK-86board to display 8888.

27. i. Interface the stepper motor with 8255 and write an ALP to control the stepper motor.
    ii. With a neat block diagram explain the operation of 8279

28. Develop an 8086 assembly language program that reads a key from the keyboard and converts it to uppercase before displaying it. The program needs to terminate on typing the 'Crtl + C' key combination.

(**Sep 06)**

29. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.
    i. Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.
    ii. Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.
    iii. Port A in mode 0, port c upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.
    iv Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. **(Sept 06)**

30. Write the necessary instruction sequence to initialize 8255 with address 0400H to 0700H for the following combinations.
    i. Port A in mode 2 and port B as input port in mode 0 without the interrupt driven i/o.
    ii. Port A in mode 2 and port B as input port in mode 1 with interrupt driven i/o.
    iii. Port A in mode 0, port c upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.
    iv. Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. **(Sept, Apr 06)**

31. i. What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2?
    ii. Explain the transistor bouncer circuit used to drive 7-segment LEDs? **(Sept 06)**

32. i. Draw the block diagram of 8255 and explain each block?
    ii. What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2? **(Sept 06)**

33. Explain why 8255 ports are divided into two groups? Discuss how these groups are controlled in different modes of operation? Explain different control signals and their associated pins for bi-directional I/O mode of operation? **(Apr 06, Nov 04)**

34. Interface a 12-bit DAC to 8255 with an address map of 0C00H to 0C03H. The DAC provides output in the range of +5V to -5V. Write the instruction sequence.
    i. For generating a square wave with a peak to peak voltage of 4V and the frequency will be selected from memory location 'F'.
    ii. For generating a triangular wave with a maximum voltage of +3V and a minimum of -2V. **(Apr 06)**

35. It is necessary to initialize interrupt for mode 1 operation of port-A as input and port-B as output in the same mode with the 8255 address map of 0400H to 0700H. Give the complete hard ware design to

interface 8255 to 8086 processor with this address map? Write the instruction sequence for the initialization of 8255 in the above modes? Give the instruction sequence to change the operation modes of port A, port C lower-half and Port B to mode 0 input ports? **(Apr 06)**

36. An 8086 system with 8255 interfaced at port A address F0H, as a block of 100 data bytes Stored in it. Another 8086 system with another 8255 interface at port A address 80H has another block of 100data bytes stored in it. Interchange this blocks of data bytes between the two 8086 systems. Draw the necessary hardware scheme and write the necessary sequence of instructions. Both systems run on the same clock rate. **(Apr 05)**

37. Interface a stepper motor with 8-step input sequence to 8086 based system and write the instruction sequence to move the stepper motor 20 steps in clockwise and 12 steps in anti-clockwise direction.

(Apr 05)

38. i. A DAC is interfaced to 8255 with an address map of 0800H to 0803H. Give the hardware design? It is necessary to design a counter type ADC with the same 8255 and DAC using a comparator. Give the necessary hardware? Provide the necessary instruction sequence to store a sample in location sample one?
    ii. Using the above hardware write the instruction sequence for successive approximation ADC? **(Apr 05)**

39. i. A DAC is interfaced to 8255 with an address map of 0B00H to 0B03H. It is necessary to design an ADC with the same 8255 and DAC using a comparator. Give the necessary hardware?
    ii. Using the above hardware write the instruction sequence for successive approximation ,ADC and counter type ADC? **(Apr 05)**

40. Explain how to interface a stepper motor with 4-step input sequence to 8086 based system with the help of hard ware design? Write the instruction sequence to move the stepper motor 10 steps in clockwise and 12 steps in anti-clockwise direction. **(Apr 05)**

41. i. Explain control word format of 8255 in I/O and BSR mode.
    ii. Interface 16 bit 8255 ports with 8086. The address of port A if F0H **(Nov 04)**

42. Explain with a block diagram how a stepper motor can be interfaced to a microprocessor and explain it working **(Nov 04)**

43. Explain the working principle of a digital-to-analog converter and how it can be interfacing. Give the hardware and software for it. **(Nov 04)**

UNIT – V

1. a) Explain the interrupt structure of 8086. What is a vector interrupt table?
   b) Explain the important features of 8259 PIC, and draw the interfacing diagram of 8259 to 8086 microprocessor. **(Nov/Dec 13)**

2. a) What is the significance of interfacing cascading of interrupt controller?
   b) Explain 8259 PIC Architecture in detail. **(Nov/Dec 13)**

3. i. Explain various DOS and BIOS interrupts. Give necessary examples.
   ii. Draw the block diagram for multiple 8259A based interrupt system. **(May 11)**

4. i. List and describe in general terms the steps an 8086 will take when it responds to an interrupt.
   ii. Explain the transfer of control for nested interrupts in 8086 with an example. **(May 11)**

5. i. Explain the interrupt response sequence of 8086 with the help of a block diagram.
   ii. Describe the purpose of 8086 interrupt vector table. **(May 11)**

6. i. With the help of the internal block diagram, explain the working of 8259 priority interrupt controller.
   ii. Explain the various hardware and software interrupts in 8086 microprocessor. **(May 11)**

7. i. Which interrupt type is associated with NMI? Mention its vector address?
   ii. What is the purpose of IF flag in handling the interrupts?
   iii. Which interrupt type is associated with TF flag? What is the vector address? Explain the use of this interrupt? **(May 09, 08, 07, Sep 06)**

8. i. Describe some important features of 8259 interrupt controller.
   ii. Distinguish between Master and Slave mode operation of 8259 **(May 09)**

9. i. Differentiate between Initialization Command Words and Operation Command Words of 8259.
   ii. Discuss about the interrupt priority schemes used in 8259. **(May 09)**

10. i. What is the difference between mask able and non-mask able interrupts. Give some examples?
    ii. Discuss about the following control word formats of 8259:
    a. Initialization Command Words (ICWs).
    b. Operational Command Words (OCW **(May 09)**

11. With detailed hardware and the associated algorithm, explain how a real time clock will be implemented in an 8086 based system. **(May 09)**

12. i. What is the interrupt vector table? Draw and explain the interrupt vector table for 8086. **(Apr 08)**
    ii. Describe the response of 8086 to the interrupt coming on INTR pin.

13. i. List out the advantages of using 8259? **(Apr 08)**
    ii. Describe the conditions that cause the 8086 to perform each of the following types of interrupts: Type-0, Type-1, Type-2 and Type-4.

14. What is an interrupt? Explain, how the 8086 processor recognizes the interrupt? Draw the timing diagram, assuming that INTR is active. Explain interrupt acknowledge cycle with its associated timing diagram. **(Apr 08)**

15. i. Which interrupt type is associated with NMI? Mention its vector address.
    ii. What is the purpose of IF flag in handling the interrupts?
    iii. Which interrupt type is associated with TF flag? What is the vector address? Explain the use of this interrupt. **(Sep 07)**

16. i. Describe the interrupt acknowledge cycle with suitable timing diagram.
    ii. Which interrupt type is associated with TF flag? What is its vector address?
    iii. What is meant by vector address? How the vector address is used to service the interrupts? **(Sep 07)**

17. i. Write an instruction sequence that will cause the priority of an 8259, Whose even address is 0800H, to be IR5, IR6, IR7, IR0, IR1, IR2, IR3, IR4. Solve this problem when the current priority is IR1 and for the second time assuming the current priority to be IR7.
    ii. Explain with examples how interrupt type-1 and type-3 provide debugging feature. **(Sep 07)**

18. Explain the following modes of operation of 8259. **(Sep 07)**
    i. Fully nested mode
    ii. Rotating priority mode
    iii. Special masked mode, and
    iv. Polled mode

19. i. Explain the interrupt structure of 8259.
    ii. Explain the operating modes of 8259.

20. i. Four sources are connected to IR lines of 8259. Emergency signal, Keyboard, A/D converter and Printer, of these, emergency signal has highest priority and the printer has lowest priority. Write all the initialization instructions. **(Sep 07)**
    ii. Write initialization instructions of 8259 PIC to meet the following specifications:
    i. Interrupt vector address: 2090 H
    ii. Call address interval of 8 bytes
    iii. Nested mode.

21. i. Describe the response that an 8259 will make if it receives an interrupt signal on its IR3 and IR5 inputs at the same time. Assume fixed priority for the IR inputs. What response will the 8259 make if it is servicing an IR5 interrupt, and an IR3 interrupt signal occurs.
    ii. Show the sequence of command words and instructions that you would use to initialize an 8259 with a base address of FF10H as follows: Edge triggered; Only one 8259; 8086 system; Interrupt Type-40 corresponds to IR0 input; Normal EOI; Non-buffered mode; Not special fully nested mode;IR1 and IR3 unmask able. **(Sep 07)**

22. i. What is the purpose of operational command words of 8259? Explain their format and the use.
    ii. Draw and explain the interrupt acknowledge cycle of 8086.

23. i. Discuss the sequence of operations performed in the interrupt acknowledge cycle?
    ii. What is the difference between RET and IRET? Discuss the result, if RET instruction is placed at the end of the interrupt service routine?
    iii. What is the vector address of type 50H interrupt? **(Sept 06)**

24. Write an initialization sequence for an 8259 that is the only 8259 in an 8086 based system, with an even address of 0F0H that will cause.
    i. Request to the edge triggered mode
    ii. IR0 request to an interrupt type 30
    iii. SP/EN to output a disable signal to the data-bus transceivers.
    iv. The ISR bits to be cleared automatically at the end of second INTA pulse.
    v. The IMR to be cleared.
    vi. The highest priority interrupt will be IR6. **(Sept 06)**

25. i. Which interrupt type is associated with NMI? Mention its vector address?
    ii. What is the purpose of IF flag in handling the interrupts?
    iii. Which interrupt type is associated with TF flag? What is the vector address? Explain the use of this interrupt? **(Sept 06)**
26. i. Write an instruction sequence that will cause the priority of an 8259, whose even address is 0200H, to be IR5, IR6, IR7, IR0, IR1, IR2, IR3, IR4. Solve this problem when the current priority is IR3 and for the second time assuming the current priority to be IR6?
    ii. Under what conditions type 0 interrupt is initiated? List out the instructions that may cause type 0 interrupt? **(Sept 06)**

27. i. How many initialization command words are required for a single 8259 in an 8086 based system? Explain their format?
    ii. Under what conditions type 0 interrupt is initiated? List out the instructions that may cause type 0 777777777interrupt? **(Apr 06, 05)**

28. Explain the following terms with reference to 8259.
    i. END of interrupt
    ii. Automatic rotation
    iii. Poll command
    iv. Read register command. **(Apr 06)**

29. i. What is minimum no. of bus cycles that can occur between the time an interrupt request is recognized and the first instruction in the interrupt routine is fetcher. Draw the bys cycles.

ii. Write an instruction sequence that will cause the priority of an 8259, whose even address is 08A0, to be IR4, IR5, IR6, IR7, IR0, IR1, IR2, IR. Solve this twice, once assuming that the highest priority is currently IR0 and once assuming that it is IR3. **(Apr 05, 04)**

30. Draw a flow chart for interrupt processing sequence and explain. **(Apr 05)**

31. Explain operational command words of 8259 with examples. **(Apr 05)**

32. What is the purpose of operational command words of 8259? Explain their format and the use? **(Apr 05)**

33. i. Write about interrupt sequence in and 8086 system.
    ii. Explain about command words of 8259
    iii. Show interfacing schematic for connecting 13 interrupting devices to 8086 using 8259. **(Nov 04)**

34. What are the steps involved in serving an interrupt by 8259 a programmable interrupt controller. **(Nov 04)**

35. Draw the interrupt vector table and explain Type0, Type1, Type2 and Type3 interrupts. **(Nov 04)**

36. i. What are the 5 types of interrupts supported on the 8086
    ii. Write about interrupt vectors? And how many bytes of memory does an interrupt vector requires.
    iii. Address 00080H in the interrupt vector table contains 4A24H, and address 00082H contains 0040H. **(Apr 04)**

37. i. To what interrupt type do these locations corresponds?
    ii. What is the starting address for the interrupt service procedure? **(Apr 04)**

38. i. Write an instruction sequence that when executed will toggle the state of the read register bit in OCW3. Assume that the 8259 is located at memory address 0A000H
    ii. How do you set or clear the interrupt flag IF? And what is its importance in the interrupt structure of 8086
    iii. How 8259 can be programmed for selecting its Interrupt request priorities. Explain. **(Apr 04)**

39. Distinguish between masking of interrupts and use of EI and DI instructions. **(Apr 04)**

40. Write the initialization instructions for the 8259 A interrupt controller to meet the following Specification.
    i. Interrupt vector address:2090H.
    ii. Call address interval of 8 digits. iii. Nested mode. **(Apr 04)**

41. i. How many initialization command words are required for a single 8259 in an 8086 based system? Explain their format?
    ii. What is type 2 interrupt? Explain the condition for initiating type 2 interrupt? What is the priority of this interrupt in 8086? **(Apr 04)**

42. Write an instruction sequence that will cause the priority of an 8259, whose even address is 0800H, to be IR5, IR6, IR7, IR0, IR1, IR2, IR3, IR4. Solve this problem when the current priority is IR1 and for the second time assuming the current priority to be IR7? **(Apr 04)**

UNIT – VI

1. a) Explain the functional pins of RS232C.
   b) How to convert RS232C to TTL conversion explain in detail. **(Nov/Dec 13)**

2. a) Distinguish between serial and parallel data transfer schemes and explain which data transfer scheme is preferred with appropriate reasons. **(Nov/Dec 13)**

   b) Interface 8251 with 8086 at address 40H. Initialize it in asynchronous transmit mode, with 7 bit character size, baud rate factor 16, one start bit, one stop bit, even parity enable. **(Nov/Dec 13)**

3. i. Show the bit pattern for the mode word and the command word that must be sent to an 8251 to initialize the device as follows: baud rate factor of 64, 7 bits/character, even parity, 1 stop bit, transmit interrupt enabled, receive interrupt enabled, and asserted, error flags reset, no hunt mode, no break character.
   ii. Brief about USB. Explain the functionality of various lines on USB. **(May 11)**

4. i. Why is synchronous serial data communication much more efficient than asynchronous communication?
   ii. Explain with a neat diagram the working of 8251 PCI. **(May 11)**

5. i. Give an overview of RS-232C serial data standard.
   ii. Draw the interface circuits for data conversion from
   (i) TTL to RS232C.
   (ii) RS 232 C to TTL. **(May 11)**

6. Interface 8251 with 8086 at address 40H. Initialize it in asynchronous transmit mode, with 7 bit character size, baud rate factor 16, one start bit, one stop bit, even parity enable. Further transmit a message "BEST OF LUCK" in ASCII from to a modem? **(May 11)**

7. i. What is the difference between 20mA current loop and RS232-C standard?
   ii. Explain the necessity of RS232 to TTL interface and draw the circuit?
   iii. Draw the circuit of TTL to RS232 and explain the necessity of this interface. **(May 09,Sep 08, Apr'07)**

8. i. Why are the two ground pins on an RS-232C connector not just tied together?
   ii. Explain the RS-232C to TTL interfacing?
   iii. Write a sequence of instructions to communicate to a modem using 8251 at address 080H. **(May 09)**

9. i. Draw the asynchronous and synchronous formats and discuss the differences.
   ii. Explain the interfacing of 8251 with 8086 with necessary circuit diagram. **(May 09)**

10. i. Discuss the types of serial communication?
    ii. Write an 8086 instruction sequence for receiving 50 characters using 8251 and store them in memory at location 2080H. **(May 09)**

11. i. What is a Status word of 8251A? Explain how 8086 processor will read the status word from 8251.
    ii. Write the sequence of instructions required to initialize 8251 at address A0H and A1H for the configuration given below:
    a. Character length - 8 bits. b. No parity c. Stop bits - 1 1/2 d. Baud rate - 16X
    e. DTR and RTS asserted f. Error flag reset. **(Apr 08)**

12. i. Explain the line driver and the line receiver circuits of serial communication. **(Apr 08)**
    ii. What do you mean by I/O mapped I/O? Draw the interfacing of 8251 with 8086 in I/O mapped I/O mode.

13. Design the hardware interface circuit for interfacing 8251 with 8086. Set the 8251 in asynchronous mode as a transmitter and receiver with even parity enabled, 2 stop bits, 8-bit character length, frequency 160 KHz and baud rate 10K:
    i. Write an ALP to transmit 100 bytes of data string starting at location 2000:5000H. **(Apr 08)**
    ii. Write an ALP to receive 100 bytes of data string and store it at 3000:4000H.

14. i. Draw and explain the null modem interfacing. **(Apr 08)**
    ii. What is Memory mapped I/O? Draw the interfacing of 8251 with 8086 in memory mapped I/O mode.

15. i. What do you mean by high-speed serial communication standard? When the high-speed serial communication standards are used?
    ii. A terminal is transmitting asynchronous serial data at 9600 baud. What is the bit time? Assuming 6 data bits, odd parity, and 2 stop bits. How long does it take to transmit one character? **(Sep 07)**

16. i. Explain the operation of 8251 in Synchronous mode of communication.

ii. Write short note on RS-232C standard. **(Sep 07)**

17. i. Explain the features of 8251 clearly. **(Sep 07)**
    ii. Explain clearly the operation of receiver section of 8251.

18. i. What are the MODEM standards? Explain why a MODEM is required to send digital data over standard telephone-lines.
    ii. Show the bit pattern for the mode word and the command word that must be sent to an 8251 to initialize the device as follows: Baud rate factor of 16, 5-bits per character, odd parity, 1 1/2 stop bits, transmit interrupt enabled, DTR and RTS asserted, Error flags reset, send break character. **(Sep 07)**

19. i. Explain the operation of 8251 in Asynchronous mode of communication.
    ii. How TTL to RS-232C and RS-232C to TTL conversions are achieved? **(Sep 07)**

20. i. What are the MODEM control lines? Explain the function of each line. Discuss how MODEM is controlled using these lines with necessary sequence of instructions.
    ii. Discuss the command instruction and status register format of 8251. **(Sep 07)**

21. i. Draw and explain the synchronous mode transmit and receive data formats of 8251.
    ii. Write a program to initialize 8251 in synchronous mode with even parity, single SYNC character, 7-bit data character. Then receive FFH bytes of data from a remote terminal and store it in the memory at address 5000H:2000H. **(Sep 07)**

22. i. Draw and explain Command and Mode word formats of 8251.
    ii. Explain the interfacing of 8251 with 8086 in memory mapped I/O mode.

23. i. Write an initialization sequence to operate 8251 in asynchronous mode with 8-bit character size, baud rate factor 64, two stop bits and odd parity enable. The 8251 is interfaced with 8086 at address 082H.
    ii. Write the instruction sequence to re-initialize the above 8251 in synchronous mode with even parity, single SYNC character and 8-bit character size? **(Apr 06, Apri 05)**

24. i. Discuss Overrun error and Framing error with reference to 8251?
    ii. Discuss the mode instruction format of 8251 for synchronous and asynchronous mode of operation?
    iii. Explain single transfer mode and block transfer mode of 8237? **(Apr 06)**

25. i. How do we connect RS-232C equipment
    i. To data terminal type devices?
    ii. To serial port of SDK -86, RS-232C connection?
    ii. Give the specifications of RS-232C. **(Apr 06)**

26. i. List out the steps involved in initializing 8251A for synchronous operation.
    ii. Give the general message format for BISYNC communication and explain. **(Apr 05)**

27. Draw necessary circuit to interface 8251 to an 8086 based system with an address 0C0H. Write the sequence of instructions to initialize 8251 for synchronous transmission? (Assume the necessary data) **(Apr 05)**

28. Write a program to initialize 8251 in synchronous mode with even parity, single SYNC character, 7 bit data character. Then receive 0FFH bytes of data from remote terminal and store it in the memory at address 2000H:2000H **(Apr 05)**

29. i. What are the MODEM control lines? Explain the function of each line? Discuss how MODEM is controlled using these lines with necessary sequence of instructions?
    ii. Discuss the Command instruction and Status register format of 8251? **(Apr 05)**

30. i. Discuss the serial data transmission standards and their specifications?

ii. A terminal is transmitting asynchronous serial data at 2400 bit. What is the bit time? Assuming 7 data bits, a parity bit and 1 stop bit how long does it take to transmit one character? **(Apr 05)**

31. i. Summarize the RS-232 C control line definitions
    ii. Describe the series of actions that DMA controller will perform after it receives a request From a peripheral device to transfer data from the device to the memory. **(Apr 05)**

32. i. Draw the block diagram of 8251 and explain each block?
    ii. Discuss the serial data transmission standards and their specifications? **(Apr 05)**

33. Interface 8251 with 8086 at address 40H. Initialize it in asynchronous transmit mode, with 7 bit character size, baud rate factor 16, one start bit, one stop bit, even parity enable. Further transmit a message " BEST OF LUCK" in ASCII from to a modem? **(Nov 04)**

34. Distinguish between synchronous and asynchronous serial data transmission techniques? Discuss the advantages and disadvantages? **(Nov 04)**

35. i. Explain Rs 232 C pin names and essential signed descriptions.
    ii. Write a short notes on 20 mA current loop. **(Nov 04)**

36. Draw the block diagram and pin description of Intel 8215 A USART **(Nov 04)**

37. i. Explain the working of 8251 I.
    ii. Give the sequence of Instructions to initialize 8251I. **(Nov 04)**

38. i. A terminal is transmitting asynchronous serial data at 1200 Bit. What is the bit time? Assuming 8 data bits, a parity bit and 1 stop bit, how long does it take to transmit one character?
    ii. Draw the flow chart showing how asynchronous serial data can be sent from a port line using a software routine.
    iii. Why are the two ground pins on an RS-232C connector not just jumper together? **(Apr 04)**

39. i. Explain the RS- 232C to TTL Interfacing.
    ii. How do we connect RS 232C equipment
    i. Connecting to 2RS232C data terminal type devices
    ii. To serial port of SDK- 86,RS – 232 C connection. **(Apr 04)**

40. Write a program to initialize 8251 in synchronous mode with even parity, single SYNCH character, 7 bit data character. Then receive FFH bytes of data from a remote terminal and store it in the memory at address 5000 H: 2000H. **(Apr 04)**

41. Interface 8251 with 8086 at an address 80H. Initialize it in asynchronous transmit mode, with 7 bit character size, band factor 16, one start bit, one stop bit, even parity enable. Further transmit a message 'HAPPY NEW YEAR' in ASCII coded form to a modem **(Apr 04)**

42. Draw the internal architecture of USART 8251 and explain its different status, mode and control word formats in detail. **(Jun 03)**

UNIT – VII

1. a) Explain the stack operation in 8051 microcontroller.
   b) How many types of addressing modes of 8051 microcontroller. **(Nov/Dec 13)**

2. a) Distinguish between virtual and protected mode and draw the memory map of the 80386 when operated in the above modes.
   b) Explain different features of Pentium architecture. **(Nov/Dec 13)**

3. Draw and explain the internal architecture of 8051 microcontroller. **(May 11)**

4. Explain the format and bit definitions of the following SFRs in 8051:
   i. TMOD,
   ii. TCON,
   iii. SCON,
   iv. IP **(May 11)**

5. Explain the salient features of 8051. **(May 11)**

6. i. Draw the architectural diagram of 8051 microcontroller and explain in detail about each block.
   ii. Explain the basic differences between a microprocessor and a microcontroller. **(May 09)**

7. i. Explain the internal RAM organization of 8051? Discuss how switching between register banks is possible? Give a sequence of instructions to switch from bank-0 to bank-2?
   ii. What is the use of SFR? List out the special function registers of 8051? **(May 09)**

8. i. Discuss the following signal descriptions: **(May 09, 07, 05, Sep 07)**
   a. (INT0)' / (INT1)'
   b. TXD
   c. T0 and T1
   d. (RD)'
   ii. Draw and discuss the formats of TMOD and PSW registers of 8051 microcontroller.

9. i. Discuss the advantages of microcontroller based system over microprocessor based systems.
   ii. Describe the following registers of 8051: **(Apr 08)**
   a. A
   b. B
   c. SP
   d. DPTR.

10. An 8051 based system requires external memory of four 8 K bytes of SRAM each and two chips of EPROM of size 4 K bytes. The EPROM starts at address 1000H. SRAM address map follows EPROM map. Give the complete memory interfacing. **(Sep 07)**

11. Draw the port pin circuits of all the ports of 8051 and explain about each port pin circuit clearly. **(Sep 07)**

12. i. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller.
   a. PCON
   b. PMOD.
   ii. Explain the stack organization of 8051 microcontroller. **(Sep 07)**

13. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?
   a. PCON b. PSW c. IP d. TMOD **(Sept, Apr 06)**

14. Discuss the following signal descriptions?
   a. ALE/PROG b. RXD c. TXD **(Sept, Apr 06, 05)**

15. Explain the support given in 8051 instruction set to handle bit addressable RAM? **(Apr 06, 05)**

16. Discuss the following signal descriptions?
   i. INT0/INT1 ii. TXD iii. T0 AND T1 iv. RD **(Apr 05)**

17. Draw and discuss the formats and bit definitions of the following SFRs in 8051 microcontroller?
   i. TMOD ii. PSW **(Apr 05)**

18. Assume that 5 BCD data items are stored in RAM location starting at 40H in 8051. Write a program to find the sum of all the numbers. The result must be in BCIV. **(Nov 04)**

19. Explain the internal architecture of 8051 with the help of a neat block diagram. **(Apr 04)**

20. List out the steps involved in programming the 8051 to transfer data serially. **(Apr 04)**

21. i. Distinguish between a microprocessor and a micro controller
    ii. Describe the hardware features of 8051 **(Apr 04)**

22. i. Write code to push R0, R1 and R3 to bank 0 into the state and pop them back into R5, R6 and R7 of bank 3 of 8051.
    ii. Write a 8051 program to find Y and Y = X2 + 2X + 5 and X is between 0 and i. **(Apr 04)**

23. Write a program to get hex data in the range of 00-FFH from port 1 of 8051 and convert into decimal. Save the digits in R7, R6 and R5 (where least significant digit is in R7). **(Apr 04)**

24. Explain the stack operation in 8051 microcontroller. **(Apr 04)**
25. Discuss how the CPU uses the stack to store CALL opcode and RET addresses. **(Apr 04)**

26. Determine whether the 8051 can be made to execute a single program instruction using external circuitry only without the help of software. **(Apr 04)**

27. Outline a scheme for single stepping the 8051 using a combination of hardware and software. **(Apr 04)**

28. Assume that ROM space of 8051 starting at 250H contains "Hello", write a program to transfer the bytes into RAM locations starting at 40H. **(Apr 04)**

29. Give the 8051-instruction format. **(Apr 04)**

30. How many ports are available in 8051? Out of them, which port pins, are individually programmable? **(Apr 04)**
31. Explain the port pin circuits for all the ports with neat diagrams. **(Apr 04)**

32. Describe the hardware features of 8051 **(Apr 04)**

33. Create a square wave of 50% duty cycle on the P1.5 bit of 8051. Timer 0 is used to generate the time delay. Analyze the program. **(Apr04)**

34. Explain the normal mode functions and alternate mode functions of different ports of 8051? Explain each pin? **(Apr 04)**

UNIT – VIII

1. a) Explain how internal memory is organized in 8051.
   b) Explain the different modes of timer in 8051. **(Nov/Dec 13)**

2. Discuss in detail Memory and I/O interfacing of 8051. **(Nov/Dec 13)**

3. Write short notes on interrupt in 8051. **(May 11)**

4. How does 8051 differentiate between the external and internal program memory **(May 11)**

5. Explain about memory and I/O addressing of 8051. **(May 11)**

6. Describe the various timer modes of operation in 8051. **(May 11)**

7. i. Explain with waveforms, the different modes of counter/timer in 8051.
   ii. Discuss in detail about parallel I/O ports in 8051 microcontroller. Also explain how these ports are accessible for specific applications. **(May 09)**

8. An 8051 based system requires external memory of four 4Kbytes of SRAM each and two chips of EPROM of size 2Kbytes. The EPROM starts at address 2000H. SRAM address map follows EPROM map. Give the complete memory interface? **(May 09)**

9. i. How does 8051 differentiate between the external and internal program memory?
   ii. Explain with waveforms different modes of counter/timer in 8051? **(May 09,Sept, Apr 06)**

10. i. How does 8051 differentiate between the external and internal program memory? **(Apr 08)**
    ii. Explain the alternate functions of Port-0, Port-2 and Port-3.
11. i. Explain various operation modes of Timer-1 and Timer-0. **(Apr 08)**
    ii. Describe the Timer control (TCON) and Timer mode control (TMOD) registers.

12. Give the complete block schematic of an 8051 based system having following specifications:
    i. 64 KB program memory
    ii. 64 KB data memory
    iii. Make use of 16 K x 8-bit memory chips and 74LS138 decoders.
    iv. Indicate clearly the address selected for the memory chips. **(Sep 07)**

13. An 8051 based system requires external memory of four 8 K bytes of SRAM each and two chips of EPROM of size 4 K bytes. The EPROM starts at address 1000H. SRAM address map follows EPROM map. Give the complete memory interface.

14. i. Enlist salient features of 8051 family of microcontrollers?
    ii. Explain with waveforms different modes of counter/timer in 8051? **(Sept 06)**

15. i. Explain the alternate functions of Port 0, Port 2 and Port 3?
    ii. Discuss the interrupt structure of 8051? Mention the priority? Explain how least priority is made as highest priority? **(Sept, Apr 06)**

16. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?
    i. PSW ii. IE iii. SCON iv.TMOD **(Sept, Apr 06, 05)**

17. Discuss the interrupt structure of 8051? Mention the priority? Explain how least priority is made as highest priority? **(Apr 06, 05)**

18. An 8051 based system requires external memory of four 8Kbytes of SRAM each and two chips of EPROM of size 4Kbytes. The EPROM starts at address 1000H. SRAM address map follows EPROM map. Give the complete memory interface? **(Apr 05)**

19. i. What is meant by interrupt. What are the different interrupt of 8051?
    ii. Explain the interrupt operation of 8051 in detail **(Nov 04)**

20. Explain the terms: **(Apr 04)**
    i. Baud rate in the 8051
    ii. SCON register
    ii. List out the steps involved in programming the 8051 to transfer data serially.

21. i. Show different methods by which a byte in TCON is copied to register R2.
    ii. Write 8051 instructions to set timer T0 to an initial setting of 1234 H. **(Apr 04)**

22. Write a program of 8051 to copy the value of 55H into RAM memory location 40H to 45H using:
    i. Direct addressing mode
    ii. Resister indirect mode without a loop
    iii. with a loop **(Apr 04)**

23. Explain 8051 communication modes with the help of suitable examples. **(Apr 04)**

24. An overrun is said to occur in data reception whenever a new byte of data is received before the previously received byte has been read. Discuss two methods by which overruns might be detected by the 8051 program. **(Apr 04)**